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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/855,660	05/16/2001	Yasuhisa Shimazaki	XA-9472	1388

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EXAMINER
CHANG, DANIEL D

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 10/18/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/855,660	SHIMAZAKI ET AL.	
	Examiner	Art Unit	
	Daniel D. Chang	2819	

-- The MAILING DATE of this communication appears n the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 August 2002 and 30 August 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24 and 37-59* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12, 14, 16, 18, 20-24, 37-59* is/are rejected.

7)☒ Claim(s) *13,15,17 and 19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Claim Objections

Claim 59 is objected to because of the following informalities: in order to have a clear antecedent basis, claim 59 should depend from 37 instead of 58. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-12, 14, 16, 18, 20-24, 37-50, and 59 are rejected under 35 U.S.C. 102(b) as being anticipated by Horiguchi et al (US 5,583,457).

Regarding claims 1-12, 16, 20-24, and 39-42, Horiguchi et al. discloses, in figure 37, a semiconductor integrated circuit comprising:

a first logic gate (L41) using, as an operation power source **in an active operation mode** (col. 1, lines 31+), a first pair of a high potential (Vcl) and a low potential (Vsl); and

a second logic gate (L43) using, as an operation power source **in an active operation mode** (col. 1, lines 31+), a second pair of a high potential (Vcc) and a low potential (Vss) having a potential difference larger than that of said first potential pair,

wherein a substrate potential of an MIS transistor (col. 3, lines 19+) in said first logic gate and that of an MIS transistor in said first logic gate and that of an MIS transistor in said second logic gate are common to each other (see substrates connected to Vcc and Vss), and

at least said first logic gate includes a p-channel type (MP41) and n-channel type (MN41) MIS transistors to which a substrate bias is applied in a reverse direction (see substrate respect to Vcl and Vsl on MP41 and MN41, respectively) by said substrate potential, and

at least said second logic gate includes a p-channel type (MP43) and n-channel type (MN43) MIS transistors to which a substrate bias is applied in a forward direction (see substrate respect to Vcc and Vss on MP43 and MN43, respectively) by said substrate potential.

Regarding claims 14 and 18, Horiguchi et al. discloses, in figure 37, that the second high potential (Vcc) is higher than the first high potential (Vcl) and the second low potential (Vss) is lower than the first low potential (Vsl), and said second high potential (Vcc) is used as a high potential side substrate potential (see substrate of MP43), and said second low potential (Vss) is used as a low potential side substrate potential (see substrate of MN43).

Regarding claims 37 and 38, for the recitation, "a design data recording medium" with "data", it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex parte Masham, 2 USPQ2d 1647 (1987).

Regarding claims 43-50 and 59, Horiguchi et al. discloses, in figure 37, that the first and second logic gates are supplied with said first and second potential pairs, respectively, as power sources in a standby mode (col. 1, lines 31+ and col. 3, lines 7+),.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 51-58 are rejected under 35 U.S.C. 103(a) as being unpatentable over Horiguchi et al.

The teachings of Horiguchi et al. have been discussed above.

Horiguchi et al. does not disclose a first potential difference as a sole operation power source and a second potential difference as a sole operation power source.

However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to omit the switches Sc and Ss to have a first potential difference as a sole operation power source and a second potential difference as a sole operation power source in order to only achieve low power consumption for semiconductor devices used in a battery-operated portable equipment and the like, since it has been held that omission of an element and its function in a combination where the remaining elements perform the same functions as before involves only routine skill in the art. *In re Karlson*, 136 USPQ 184

Response to Arguments

Applicant's arguments filed August 30, 2002 have been fully considered but they are not persuasive.

Applicant argues, on pages 8-9 of the Amendment filed August 30, 2002, that "the switches Ss and Sc are closed in the active operation mode so that the circuits L41 and L43 utilize the same potential difference (Vcc-Vss) as an operation power source, the additional potentials via resistors Rc and Rs being utilized only in the standby (low power consumption)

mode. However, the low power consumption mode does not mean that it is only a standby mode. It could also mean that the low power consumption mode is also an active operation mode for semiconductor devices used in a battery-operated portable equipment and the like (see col. 1, lines 19+). Therefore, amended claims 1-12, 14, 16, 18, 20-24, 37-42 and newly added claims 43-50 and 59 are rejected as discussed above.

Allowable Subject Matter

Claims 13, 15, 17, and 19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an examiner's statement of reasons for allowance:

The closest prior art of record, Horiguchi et al., taken alone or in combination of other references, does not teach or fairly suggest a semiconductor integrated circuit comprising, among other things, a first substrate potential which is between the first and second high potentials and a second substrate potential which is between the first and second low potentials, as set forth in the claims.

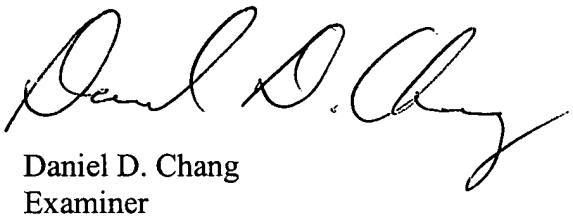
Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel D. Chang whose telephone number is (703) 306-4549. The examiner can normally be reached on Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael J. Tokar can be reached on (703) 305-3493. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.



Daniel D. Chang
Examiner
Art Unit 2819

DC
October 17, 2002

DANIEL CHANG
PRIMARY EXAMINER